This listing of claims will replace all prior versions, and listings, of claims in the present application:

LISTING OF THE CLAIMS:

Claim 1 (Currently Amended) A method of fabricating a heterobipolar transistor comprising:

forming a pedestal atop a structure that comprising at least a base layer located on a surface of a substrate having a collector and trench isolation regions located therein, ~~wherein said base layer is monocrystalline over the collector and polycrystalline over the trench isolation regions~~;

forming an extra base layer over said structure including said pedestal, wherein said extra base layer comprises monocrystalline material over the substrate and polycrystalline material over the pedestal and said base layer that is located atop said trench isolation regions ~~polycrystalline~~, said polycrystalline material over said pedestal is thinner than the polycrystalline material over said base layer that is located atop said trench isolation regions ~~polycrystalline~~;

converting at least said polycrystalline material over said pedestal of said extra base layer into an oxide utilizing a low temperature process that is performed at a temperature of about 700°C or less;

removing said oxide and said pedestal from said structure to provide an emitter opening; and

forming at least a polysilicon emitter in said emitter opening.

Claim 2 (Original) The method of Claim 1 wherein said pedestal is an oxide pedestal that is formed by deposition, lithography and etching.

Claim 3 (Original) The method of Claim 2 wherein said removing of said oxide formed by said converting step and said oxide pedestal are performed using a single etching step and some polycrystalline material of said extra base layer remains.

Claim 4 (Original) The method of Claim 3 further comprising forming an oxide layer in at least said emitter opening after said removal step.

Claim 5 (Original) The method of Claim 4 wherein said oxide layer is formed by a low temperature oxidation process that is performed at a temperature of about 700°C or less.

Claim 6 (Original) The method of Claim 5 wherein said low temperature oxidation is a high-pressure oxidation process that is performed at a pressure of about 1 atmosphere or greater.

Claim 7 (Original) The method of Claim 4 further comprising forming a nitride spacer on each exposed sidewall within said emitter opening.

Claim 8 (Original) The method of Claim 7 further comprising performing a chemical oxide removal process to remove said oxide layer from a bottom surface of said emitter opening thereby exposing the base layer.

Claim 9 (Original) The method of Claim 8 wherein said chemical oxide removal process is a vapor or a plasma of HF and NH_3.

Claim 10 (Original)The method of Claim 1 wherein said base layer is formed by an epitaxy growth process that is performed at a temperature from about 450°C to about 700°C.

Claim 11 (Original) The method of Claim 1 wherein said base layer comprises Si, SiGe or a combination of Si and SiGe.

Claim 12 (Original) The method of Claim 1 wherein said structure further comprises an optional Si-containing cap layer located atop said base layer.

Claim 13 (Original) The method of Claim 1 wherein said forming said extra base layer comprising an epitaxy growth process that is performed at a temperature from about 450°C to about 700°C.

Claim 14 (Original) The method of Claim 1 wherein said extra base layer comprises Si, SiGe or a combination of Si and SiGe.

Claim 15 (Original) The method of Claim 1 wherein said low temperature oxidation process comprises a high-pressure oxidation process that is performed at a pressure of about 1 atmosphere or greater.

Claim 16 (Original) The method of Claim 1 wherein said removing step comprises an etching process that selectively removes oxide.

Claim 17 (Original) The method of Claim 1 wherein said forming at least said polysilicon emitter comprising depositing a doped or undoped polysilicon layer, optionally implanting dopants into said undoped polysilicon layer, lithography and etching.

Claims 18-23 (Cancelled)

Claim 24 (Currently Amended) A method of forming a heterobipolar transistor comprising the steps of:

forming an oxide pedestal atop a structure that comprising at least a base layer located on a surface of a substrate having a collector and trench isolation regions located therein, ~~wherein said base layer is monocrystalline over the collector and polycrystalline over the trench isolation regions~~;

forming an extra base layer over said structure including said oxide pedestal, wherein said extra base layer comprises monocrystalline material over the substrate and

polycrystalline material over the oxide pedestal and said base layer that is located above said trench isolation regions ~~polycrystalline~~, said polycrystalline material over said oxide pedestal is thinner than the polycrystalline material over said base layer that is located above said trench isolation regions ~~polycrystalline~~;

converting at least said polycrystalline material over said oxide pedestal of said extra base layer into an oxide utilizing a low temperature oxidation process;

removing said oxide and said oxide pedestal from said structure using a single etching process to provide an emitter opening;

forming an oxide layer on exposed surfaces using a second low temperature oxidation process;

forming a nitride spacer within said opening;

removing said oxide layer from a bottom surface of said emitter opening exposing said base layer; and

forming at least a polysilicon emitter in said emitter opening.

Claims 25-26 (Cancelled)